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2.36” TFT LCD MODULE SPECIFICATION

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1 GENERAL DESCRIPTION

1.1 Description

- ✓ Screen size: 2.36 inch diagonal
- ✓ Number of dots displayed: 112,320 dots
- ✓ Display mode: Normally white / Transmissive
- ✓ One chip solution with COG mounting
- ✓ DC2DC power supplies (VGH/VGOFFL/VCOM voltage supply).
- ✓ Support 8-bit digital (RGB) or CCIR_601/656 input timing
- ✓ Incorporated white LED back light unit (serial type)

1.2 Physical specification

No.	Item	Specification	UNIT
1	Number of Dots	480 (W) x 234 (H)	dot
2	Display Size (Diagonal)	2.36 (5.98 cm)	Inch
3	Dot Pitch	0.10(W) x 0.1525 (H)	mm
4	Active Area	48.0 x 35.685	mm
5	Viewing Angle	6 O'clock	-
6	Color Arrangement	R.G.B. delta	-
7	Dimension (W x H x D)	55.2 x 47.55 x 2.9 The protrusions (FPC, parts) are excluding.	mm
8	Surface Treatment	Anti-glare(AG), Hard-coating	
9	Weight	T.B.D.	g

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2 ABSOLUTE MAXIMUM RATINGS

2.1 Absolute maximum ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage (1)	VDD1	-0.3 to +7.0	V	
Power Supply Voltage (2)	VDD2	-0.3 to +7.0	V	
Power Supply Voltage (3)	PCDD	-0.3 to +7.0	V	
Logic Output Voltage	Vout1	-0.3 to +7.0	V	
Input Voltage	Vin	-0.3 to VDD+0.3	V	

Note:

- (1) All of the voltages listed above are with respect to VSS=0V.
- (2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

2.2 Environmental absolute maximum ratings

Item	Symbol	Min.	Max.	unit	Note
Storage Temperature	Tstg	(-55)	(125)	°C	(1)
Operating Temperature (Ambient Temperature)	Topr	(-30)	(85)	°C	(1),(2)

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3 Electrical characteristics

3.1 Typical operating conditions (GND=AVss =0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply voltage	VDD1	2.7	3.3	3.6	V	
	VDD2	2.7	3.3	3.6	V	
	PVDD	3.0	3.3	3.6	V	
Analog Standby current	I _{STBY3}	-	-	10	uA	
Input Signal Voltage	H Level	V _{IH}	0.7V _{cc}	-	V _{cc}	V
	L Level	V _{IL}	GND	-	0.3V _{cc}	V

3.2 Backlight driving conditions (LED)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I _L		20	30	mA	Note 1
LED voltage	V _L	9.0	10.2	11.4	V	

Note 1: LEDs are in serial type.

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4 AC CHARACTERISTICS

4.1 Timing conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Delay between Hsync and DCLK	Thc	-	-	1	DCLK
Hsync width	Twh	1	32	-	DCLK
Hsync period	Th	60	63.5	67	ns
Vsync setup time	Tvst	12	-	-	ns
Vsync hold time	Tvhd	12	-	-	ns
Hsync setup time	Thst	12	-	-	ns
Hsync hold time	Thhd	12	-	-	ns
Data set-up time	Tdsu	12	-	-	ns
Data hold time	Tdhd	12	-	-	ns
DE set-up time	Tesu	12	-	-	ns
Vsync width	Twv	2	4	6	Th
Vsync period NTSC	Tv	-	262.5	-	Th
Vsync period PAL	Tv	-	312.5	-	Th
Hsync to Vsync time for ODD field	T_{HVO}	-4		+4	DCLK
Hsync to Vsync time for EVEN field	T_{HVE}	-	0.5	-	Th
SD output stable time	Tst	-	-	30	μ s
GD output stable time	Tgst	-	1	-	μ s
Serial communication					
Serial clock period	Tsck	320	-	-	ns
Serial clock duty cycle	Tscw	40	50	60	%
Serial clock width	Tssw	120	-	-	ns
Serial data setup time	Tist	120	-	-	ns
Serial data hold time	Tihd	120	-	-	ns
SPENB setup time	Tcst	120	-	-	ns
SPENB data hold time	Tchd	120	-	-	ns
Chip select distinguish	Tcd	1	-	-	us
Delay between SPCK and Vsync	Tcv	1	-	-	us

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4.2 Operating mode dependent AC characteristic

Serial RGB mode, SEL[2...0]=[000,001]

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk	-	9.7	-	Mhz
DCLK period	Fcph	-	103	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso	-	56	-	DCLK
Delay from Hsync to Gate output	Thgo	-	45	-	DCLK
Delay from Hsync to Gate output off	Thgz	-	19	-	DCLK
Delay from Hsync to FRP	Thf	-	56	-	DCLK
Delay from Hsync to 1,st data input (for SYNC mode)	Ths	84	100	115	DCLK

4.3 Operating mode dependent AC characteristic

YUV mode, SEL[2...0]=[010~101]

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk	-	24.54/27	-	Mhz
DCLK period	Fcph	-	40.7/37	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso	-	143	-	DCLK
Delay from Hsync to Gate output	Thgo	-	113	-	DCLK
Delay from Hsync to Gate output off	Thgz	-	48	-	DCLK
Delay from Hsync to FRP	Thf	-	143	-	DCLK
Delay from Hsync to 1,st data input (for TS601=0)	Ths	233	249	264	DCLK

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4.4 Operating mode dependent AC characteristic

CCIR656 mode, SEL[2...0]=[110]

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk	-	27	-	Mhz
DCLK period	Fcph	-	37	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from CCIR_H to Source output	Thso	-	171	-	DCLK
Delay from CCIR_H to Gate output	Thgo	-	141	-	DCLK
Delay from CCIR_H to Gate output off	Thgz	-	76	-	DCLK
Delay from CCIR_H to FRP	Thf	-	171	-	DCLK

4.5 Operating mode dependent AC characteristic

CCIR656 mode, SEL[2...0]=[111]

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk	-	24.54	-	Mhz
DCLK period	Fcph	-	40.7	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from CCIR_H to Source output	Thso	-	171	-	DCLK
Delay from CCIR_H to Gate output	Thgo	-	141	-	DCLK
Delay from CCIR_H to Gate output off	Thgz	-	76	-	DCLK
Delay from CCIR_H to FRP	Thf	-	171	-	DCLK

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5 OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in note (1).

Measuring equipment: BM-5A, BM-7

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise	Tr	$\theta = 0^\circ$	-	15	30	ms	Note 4
Fall	Tf		-	35	50	ms	
Contrast ratio	CR	At optimized viewing angle	150	200	-		Note 5,6
Viewing angle Top		$CR \geq 10$	-	40	-	deg.	Note 7
Bottom			-	60	-		
Left			-	50	-		
Right			-	50	-		
Brightness	B	$\theta = 0^\circ$	180	200	-	nit	Note 8
White chromaticity	x	$\theta = 0^\circ$	-	(0.29)	-		
	y	$\theta = 0^\circ$	-	(0.29)	-		
Degree of Saturation (NTSC)			-	50	-	%	

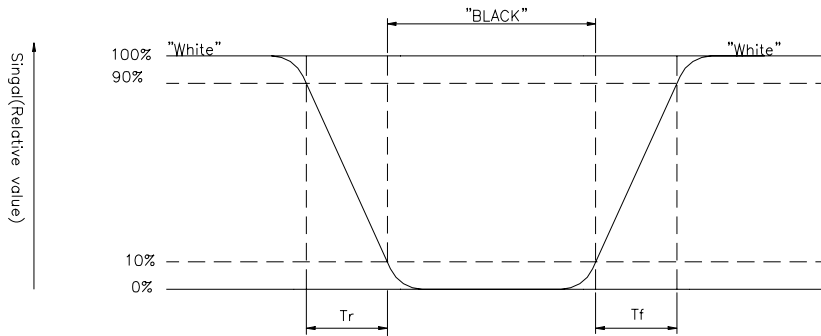
Note 1: Ambient temperature =25°C, And LED current IL=20mA.

Note 2: To be measured in the dark room.

Note 3: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 4: Definition of response time: The output signals of photo-detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black” (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as shown below.

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Note 5: Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo-detector output when LCD is at "White" state}}{\text{Photo-detector output when LCD is at "Black" state}}$$

Note 6: White $V_i = V_{i50} + 1.5V$
 Black $V_i = V_{i50} \pm 2.0V$

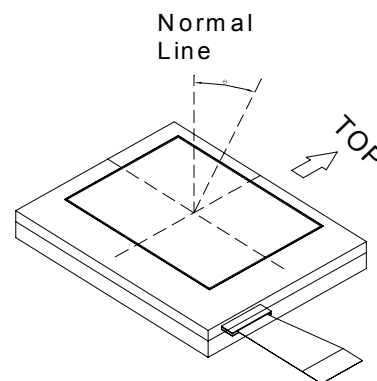
“±” means that the analog input signal swings in phase with VCOM signal.

“∓” means that the analog input signal swings out of phase with VCOM signal.

“ V_{i50} ” : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

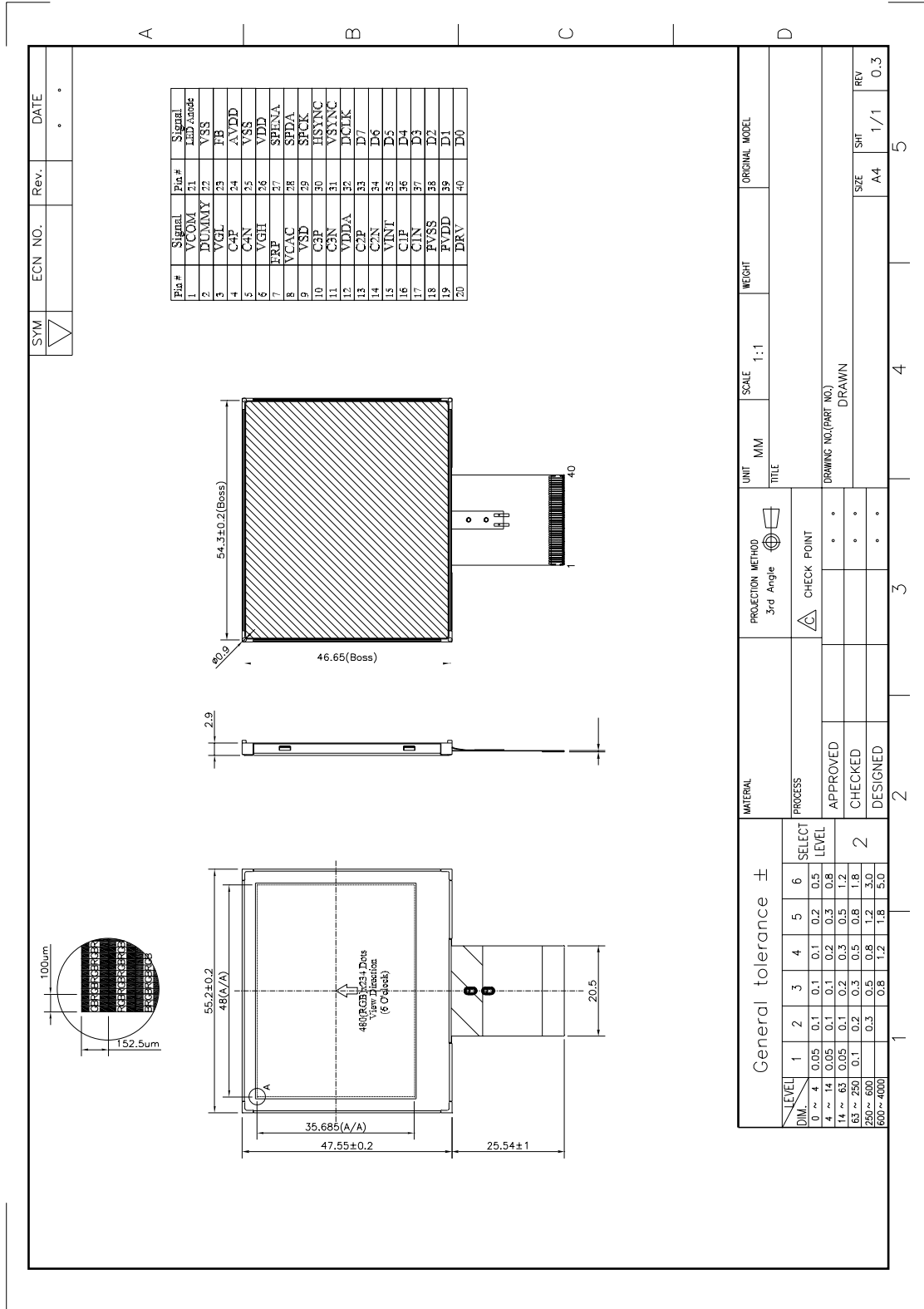
Note 7: Definition of viewing angle:
 Refer to figure as below.



Note 8: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

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6 OUTLINE DIMENSION



General tolerance ±		MATERIAL		PROJECTION METHOD		UNIT		SCALE		WEIGHT		ORIGINAL MODEL	
LEVEL		PROCESS		3rd Angle		MM		1:1					
D.M.		APPROVED		CHECK POINT		TITLE		DRAWING NO.(PART NO.)		SIZE		REV	
0 ~ 4	0.05	1	0.1	2	0.1	3	0.1	4	0.2	5	0.5	A4	1/1
4 ~ 14	0.05	1	0.1	2	0.2	3	0.3	4	0.5	5	0.8		0.3
14 ~ 63	0.05	1	0.1	2	0.3	3	0.5	4	0.8	5	1.2		
63 ~ 250	0.1	1	0.2	2	0.5	3	0.8	4	1.2	5	1.8		
250 ~ 630	0.15	1	0.3	2	0.8	3	1.2	4	2.0	5	3.0		
630 ~ 4000	0.2	1	0.5	2	1.2	3	1.8	4	3.0	5	4.5		

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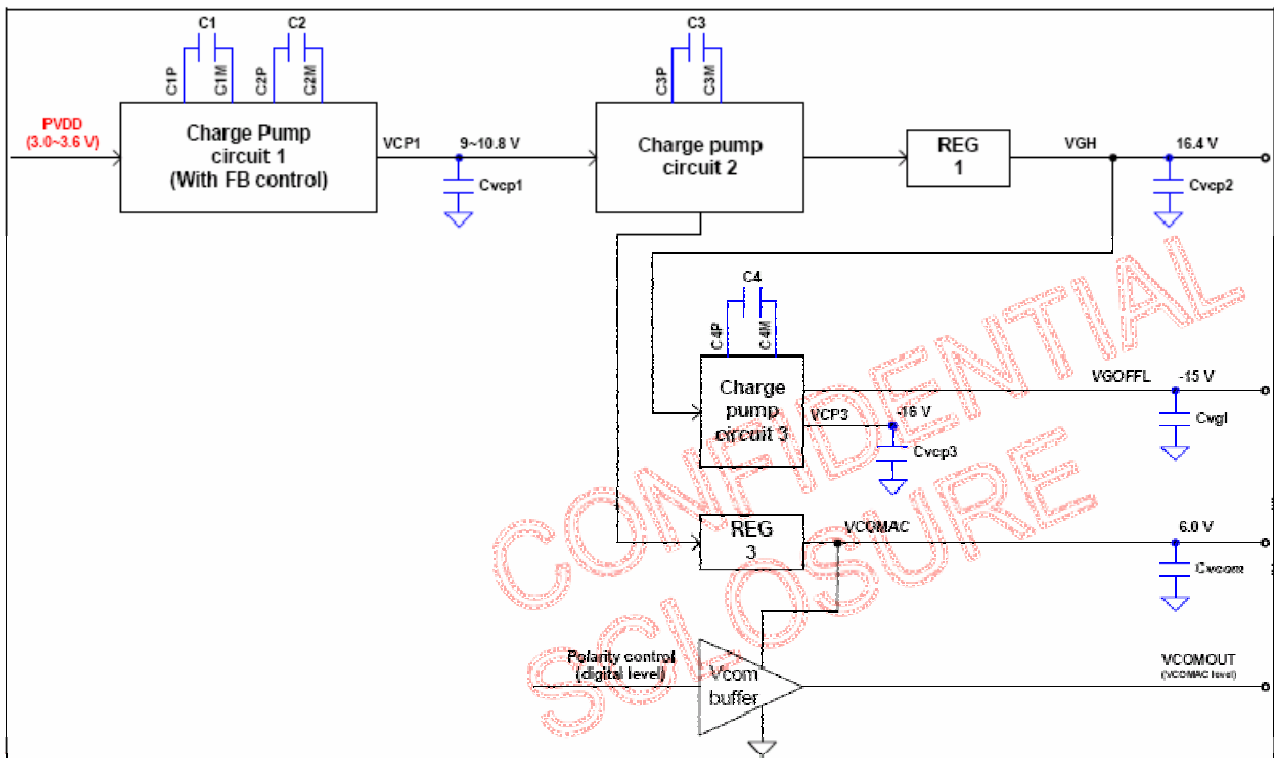
7 INTERFACE PIN CONNECTION

Pin No.	Symbol	I/O	Description
1	VCOM	I	Common electrode driving voltage
2	DUM	-	Dummy pads. For CS on Gate use only.
3	VGOFFL	PS	Negative power supply for gate driver output
4	C4P	C	Capacitor connect pin for internal charge pump. Refer to "Power Circuit" for the application.
5	C4M	C	
6	VGH	PS	Positive power supply for gate driver output
7	VCOMOUT	O	Frame polarity output for panel VCOM
8	VCOMAC	C	Power supply for VCOMOUT output
9	VCP3	C	Capacitor connect pin for internal charge pump. Refer to "Power Circuit" for the application.
10	C3P	C	Pins to connect capacitance for power circuit
11	C3M	C	
12	VCP2	C	
13	C2P	C	
14	C2M	C	
15	VCP1	C	
16	C1P	C	
17	C1M	C	
18	PGND	PI	Ground pins for charge pump circuits
19	PVDD	PI	Power supply for charge pump circuits
20	DRV	PO	Gate signal for the power transistor of the boost converter
21	LED Anode	I	For LED analog voltage
22	GND	PI	Ground pins for digital circuits
23	FB	P	Main boost regulator feedback input

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24	AVDD	PI	Power supply for analog circuits
25	GND	PI	Ground pins for digital circuits
26	VCC	PI	Power supply for digital circuits
27	SPENB	I	3-Wire communication enable. Active low.
28	SPDA	I/O	3-Wire communication data input / output
29	SPCK	I	3-Wire communication clock input
30	HSD	I	Horizontal sync input
31	VSD	I	Vertical sync input
32	CLKIN	I	Clock signal for input data
33	DIN7	I	Data input: MSB
34~39	DIN6~ DIN1	I	Data input
40	DIN0	I	Data input: LSB

Note: I: Input; O: Output; P: Power; PO: Power output; C: Capacitor pin; PS: Power setting;
I/O: Input/output



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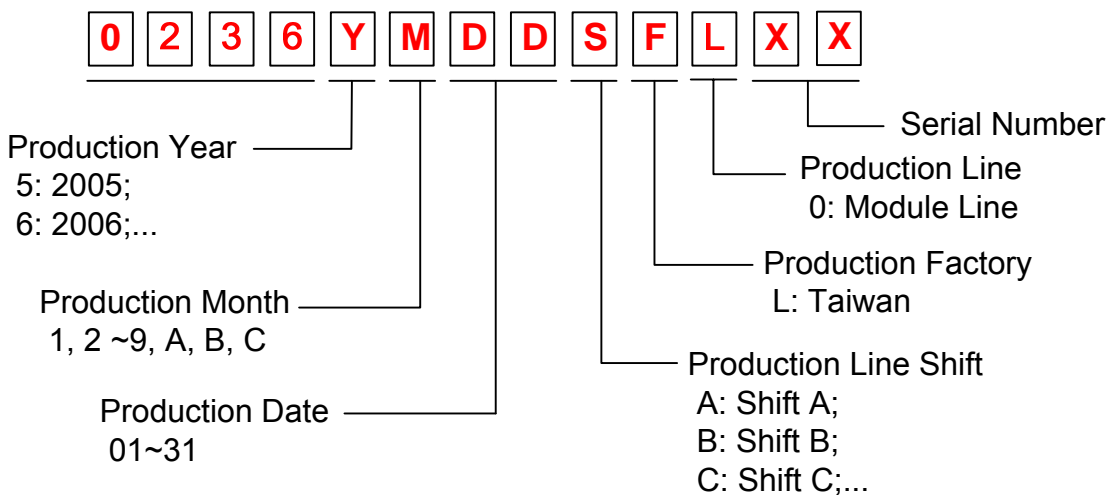
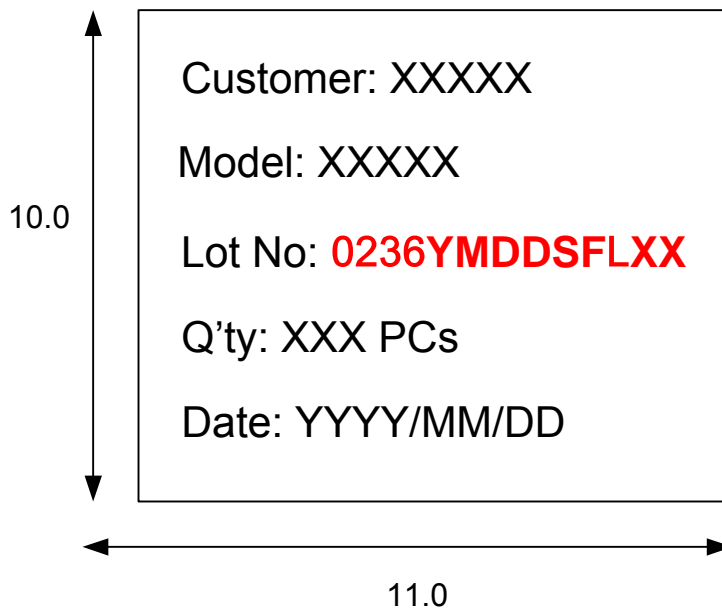


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9 DESIGNATION OF LOT MARK

9.1 Lot Mark on Packing Label

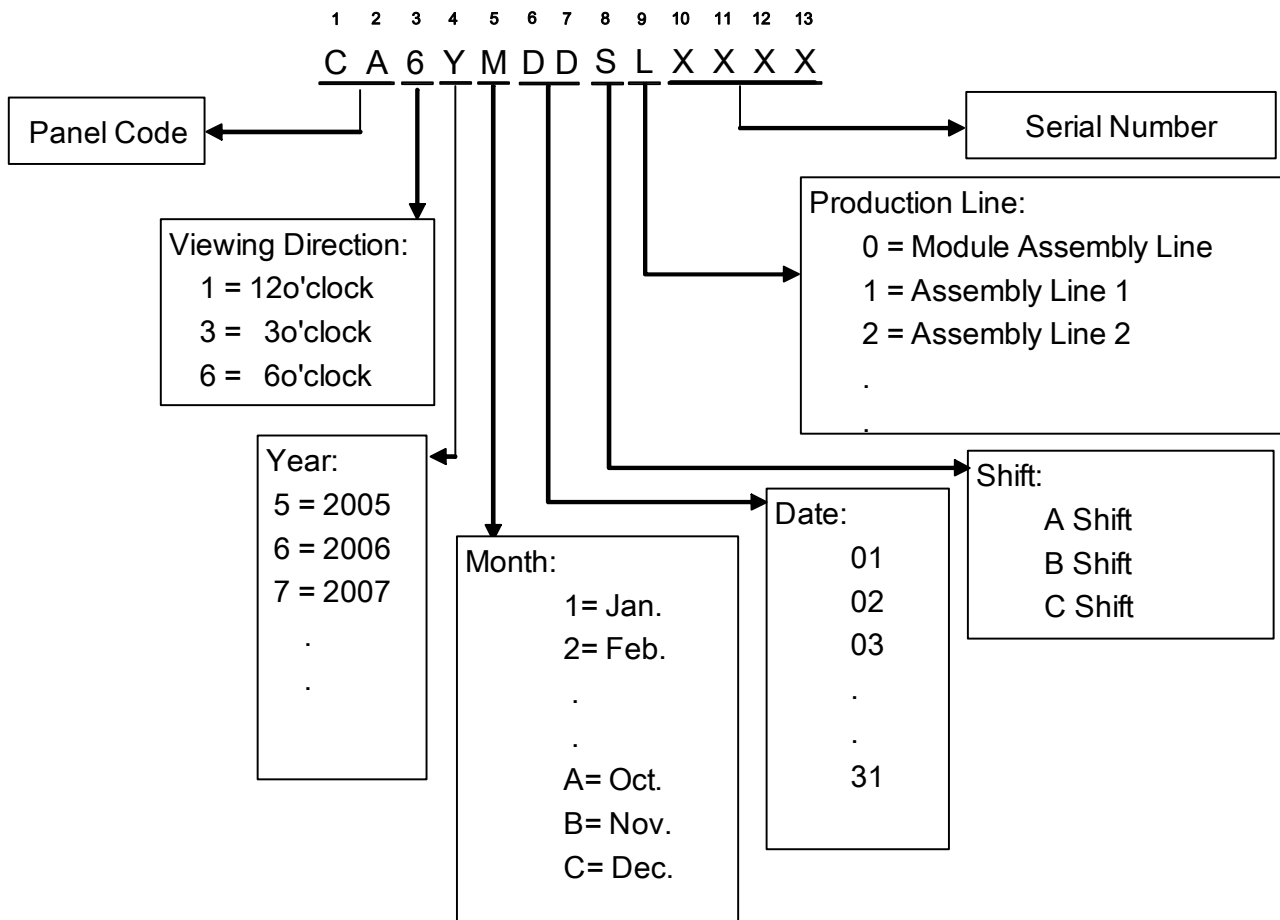
Lot Number on Outer
Carton Box



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9.2 Production Lot Mark of LCD Module

The production lot of module is specified on the back of FPC follows. The lot mark is consisted of 13-digit number.



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10 RELIABILITY DATA

No	Test items	Conditions	Remark
1	High temperature storage	Ta=80°C 240Hrs	
2	Low temperature storage	Ta= -25°C 240Hrs	
3	High temperature operation	Ta= 60°C 240Hrs	
4	Low temperature operation	Ta=0°C 240Hrs	
5	High temperature and high humidity	Ta=60°C , 90%RH 240Hrs	Operation
6	Thermal shock	-25°C ~ 80°C/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V, 200pF(0Ω), once for each terminal	Non-operation
8	Vibration (with carton)	Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges ,6 surfaces	

Note: Ta: Ambient temperature.

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11 PRECAUTIONS

11.1 Handling

- (1) When the module is assembled, it should be attached to the system firmly. Be careful not to twist and bend the module.
 - (2) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
 - (3) Note that the polarizer is very fragile and could be easily damaged. Do not press or scratch the surface harder than a B pencil lead.
 - (4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining and discoloration may occur.
 - (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
 - (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Don't use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
 - (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
 - (8) Protect the module from static; it may cause damage to the CMOS Gate Array IC.
 - (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
 - (10) Do not disassemble the module.
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- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.

11.2 Storage

- (1) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%.
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

11.3 Operation

- (1) Do not connect; disconnect the module in the "Power on" condition.
- (2) Power supply should always be turned on/off by the chapter 8 TFT-LCD Driver IC Operation Algorithms.

11.4 Others

- (1) The Liquid crystal is deteriorated by ultra violet, do not leave it in direct sunlight and strong ultraviolet ray for many hours.
 - (2) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
 - (3) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation in part contents and environmental temperature and so on). Otherwise the panel may be damaged.
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- (4) If the panel displays the same pattern continuously for a long period of time, it can be the situation when the image "Sticks" to the screen.
- (5) His panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

